Serial No.10/769,127 HP Docket No: 200209576-1

REMARKS

This communication is in response to the Office Action dated July 11, 2006. Claims 1-10, 13-20, 22 and 23 are pending in the present Application.

Claims 11, 12, 21 and 24-30 have been withdrawn from consideration. Claims 1-10, 13-20, 22 and 23 are rejected.

§102 Rejections

Claims 1-10, 13-20, 22 and 23

For ease of review, Applicant reproduces independent claims 1 and 13 herein below:

- A method for forming a semiconductor device comprising:
 forming a 3-dimensional (3D) pattern in a substrate; and
 depositing at least one material over the substrate in accordance with
 desired characteristics of the semiconductor device.
- 13. A system for forming a semiconductor device comprising: means for forming a 3-dimensional (3D) pattern in a substrate; and means for depositing at least one material over the substrate in accordance with desired characteristics of the semiconductor device.

The Examiner states:

Claims 1-10, 13-20 and 22-23 are rejected under 35 USC §102(e) as being anticipated by Taussig et al. (US 6,861,365).

Applicant respectfully disagrees. The present invention includes a method and system for forming a semiconductor device. Varying embodiments allow 2-

Serial No.10/769,127 HP Docket No. 200209576-1

dimensional alignment features to be created in 3-dimensional structures on a device substrate prior to any processing steps. Subsequent processing steps, including material deposition, planarization and anisotropic etching are utilized to construct a multi-level aligned pattern. Accordingly, the use of the method and system can potentially increase the flexibility of the semiconductor manufacturing process.

Claim 1 recites a method for forming a semiconductor device that includes forming a 3-dimensional (3D) pattern in a substrate and depositing at least one material over the substrate in accordance with desired characteristics of the semiconductor device.

The Examiner states that the Taussig reference anticipates the present invention. Applicant respectfully disagrees and asserts that the Taussig reference does not disclose forming a 3-dimensional (3D) pattern in a substrate as recited in claim 1 of the present invention. (Emphasis added.) Taussig discloses a method and system for forming a semiconductor device. The method and system involves the utilization of a stamping tool to generate three-dimensional resist structures whereby thin film patterning steps can be transferred to the resist in a single molding step and subsequently revealed in later processing steps.

Applicant herein asserts that the present invention recites the formation of 3D patterns in a substrate whereas the Taussig reference discloses the implementation of a stamping tool to transfer patterns into a resist structure on a substrate. (Emphasis added.) The present invention recites the formation of 3D structure in a substrate. Applicant accordingly asserts that the formation of 3D patterns in a substrate is clearly different from the implementation of a stamping

Serial No.10/769,127 HP Docket No. 200209576-1

tool to transfer patterns into a resist structure on a substrate. Consequently,

Applicant contends that the Taussig reference does not disclose the formation of

3D patterns in a substrate as recited in claim 1 of the present invention.

Since the Taussig reference does not disclose the formation of 3D patterns in a substrate as recited in claim 1 of the present invention, claim 1 of the present invention is allowable over the Taussig reference. Furthermore, claim 12 discloses similar features of claim 1 and should also be deemed allowable over the Taussig reference.

Claims 2-10, 13-20 and 22-23

Since claims 2-10, 13-20 and 22-23 are respectively dependent on claims 1 and 13, the above-articulated arguments with regard to independent claims 1 and 13 apply with equal force to claims 2-10, 13-20 and 22-23. Accordingly, claims 2-10, 13-20 and 22-23 should be allowed over the Examiner's cited reference.

Serial No. 10/769, 127 HP Docket No: 200209576-1

Applicant believes that this application is in condition for allowance.

Accordingly, Applicant respectfully requests reconsideration, allowance and passage to issue of the claims as now presented. Should any unresolved issues remain, Examiner is invited to call Applicant's attorney at the telephone number indicated below.

Respectfully submitted,

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